(Pages : 3) **1504**

Reg. No. : .....

Name : .....

Sixth Semester B.Tech. Degree Examination, May 2012
(2008 Scheme)
Branch : Computer Science and Engg.
08.605 : HIGH PERFORMANCE MICROPROCESSORS

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **4** marks.

1. Explain the following 80286 instructions.
   i) LGDT ii) LAR
   iii) LSL iv) VERW.

2. What are the different checks performed by 80386 when an attempt is made to access a segment by loading a segment selector into the visible part of the segment register ?

3. Describe how two integer units allow Pentium to execute two non-dependent instructions simultaneously.

4. What are the features of Advanced Transfer Cache of pentium 4 ?

5. List out the characteristics of RISC machines.

6. Give the sizes of the following of MIPS R4000 :
   i) Physical memory ii) Virtual address
   iii) Virtual memory iv) Secondary cache.

7. What you meant by banked registers ?

8. Differentiate between a micro processor and a micro controller.

9. Explain the Program Status Word (PSW) of 8051.

10. What is the purpose of Instruction Command Code register and data register of LCD ? How are they selected ?

P.T.O.

PART – B

Answer **one full** question from **each** Module. **(3×20=60 Marks)**

Module – I

11. a) With a neat block diagram explain the functional parts of 80286 microprocessor. **12**

    b) Differentiate between segment descriptors and system descriptors ? Draw and explain the structure of an 80386 segment descriptor. **8**

OR

12. a) Briefly explain the architecture of Pentium Pro with a neat block diagram. **12**

    b) What do you mean by out-of-order execution ? Explain the functions of out-of-order execution engine of Pentium 4. **8**

Module – II

13. a) Explain the compiler based register optimization techniques in RISC machines. **10**

    b) Briefly explain RISC pipelining. **10**

OR

14. a) Explain the following ARM instructions. Which of them would cause the assembler to issue a syntax error message ? Why ?

    i) ADD R_2, R_2, R_2.

    ii) SUB R_0, R_1, [R_2, #4]

    iii) MOV R_0, #2 – 1010101

    iv) MOV R_0, # 257

    v) ADD R_0, R_1, R_{11}, LSL #8. **10**

    b) Explain the register organization and modes of operations of ARM. **10**

Module – III

15. a) Briefly explain the architecture of 8051 with a block diagram. 13

    b) Explain the addressing modes of 8051 with examples. 7

OR

16. a) Explain the format of IE and IP registers of 8051 ? 6

    b) Describe the pins of LCD. 7

    c) Describe briefly how a micro controller detects and identifies a key pressed on a key board. 7